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Editorial

FPGA-based reconfigurable computing II

This "Special Issue on FPGA-based Reconfigurable Computing" presents a collection of high-quality papers from the FPGA research community. The 23 accepted papers were selected from the 74 submissions received from 14 countries. These 23 accepted papers are arranged to be published in three issues. In the first issue of the three-issue series, we have published 8 papers in Volume 30, Issue 6, 2006.

In this second issue, we include eight papers that cover a spectrum of FPGA-based reconfigurable computing. The topics covered in the papers are related to the issues of using FPGA-based reconfigurable computing in various applications. The authors have done an excellent job of presenting the material. We are sure this issue will be very informative for all the readers who are engaged in FPGA-based reconfigurable computing.

The title of our first paper is "Secure IP Downloading for SRAM FPGAs," by J. Castillo, P. Huerta, J.I. Martinez. This paper presents a review of the methods of secure IP downloading and rights management in FPGA systems. This research proposes to use self-reconfiguration for local security, encryption protocols for a secure remote updating, and right management for the server side. A complete system that allows Secure IP downloading was demonstrated in the paper.

The second paper, entitled "An Improved Algorithm for Assessing the Overall Quantization Error in FPGA Based CORDIC Systems Computing A Vector Magnitude," by S. W. Alexander and R. W. Stewart, presents a study on the accuracy of CORDIC algorithm which can be used to compute arithmetic functions. Then, this paper presents a more accurate equation for the Overall Quantization Error (OQE). This equation can lead to a more efficient architecture which uses fewer FPGA resources.

The title of our third paper is "Reconfigurable system for high-speed and diversified AES using FPGA," by M.H. Jing, Zih-Heng Chen, Jian-Hong Chen, and Y.H. Chen. This paper presents a FPGA-based implementation of Advanced Encryption Standard (AES) algorithm. The proposed design uses look-up tables (LUTs) based system core for encryption and decryption. Finally, a function generator that calculates and produces the content of the downloadable LUTs is presented.

The forth paper, entitled "Optimized High-order Finite Difference Wave Equations Modelling On Reconfigurable Computing Platform," by Chuan He, Guan Qin, Mi Lu, and Wei Zhao, proposes to accelerate the execution of wave field modeling problem on reconfigurable computing platform. The idea is to adopt high-order temporal and spatial Finite Difference schemes and a proposed on-chip data buffering structure. An implementation that achieves better price-performance ratio and lower power consumption is also reported.

The title of our fifth paper is "An Automated, FPGA-based Reconfigurable, Low-Power RFID Tag," by Alex K. Jones, Raymond Hoare, Swapna Dontharaju, Shenchih Tung, Ralph Sprang, Josh Fazekas, James T. Cain, and Marlin H. Mickle. This paper reports an automated design flow that creates customized, low-power, active RFID tags. It also presents two implementation strategies. Performance and power consumption in various implementations (e.g., ASIC and FPGA) are also reported in this paper.

The sixth paper "Families of FPGA-Based Accelerators for Approximate String Matching," by Tom Van Court, and Martin C. Herbordt intends to find a FPGA-based accelerator that can address different parts of the approximate string matching problem. The proposed methods can make maximum use of the FPGA fabric. Speed-ups in the range of 150× to 400× over a PC are also reported.

The seventh paper, "A Wire Delay-Tolerant Reconfigurable Unit for a Clustered Programmable-Reconfigurable Processor" by Richard B. Kujoth, Chi-Wei Wang, Jeffrey J. Cook, Derek B. Gottlieb and Nicholas P. Carter, deals with the design of the reconfigurable clusters on the clustered programmable-reconfigurable processor. The proposed strategies include using pipeline registers at the intersections between wires, retiming buffers and register queues. This paper reports performance gain based on proposed schemes over a purely-programmable processor.

The last but not least important paper in this issue, "FPGA Architecture for Fast Parallel Computation of Co-occurrence Matrices," by D.K. Iakovidis, D.E. Maroulis,

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and D.G. Bariamis, presents an architecture design for fast parallel computation of co-occurrence matrices in high throughput image analysis applications. The proposed architecture was implemented on FPGA using VHDL. The performance of proposed design is compared to a software implementation running on a general purpose processor.

We hope that these research papers will help to give a better insight into the latest trend of works on the critical issues of FPGA-based reconfigurable computing. We take this opportunity to thank all the authors who have submitted their papers for this special issue and also the reviewers who spend their valuable time in reviewing the papers and providing constructive comments. Without their participation, it would have been difficult for us to meet the deadlines.

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